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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	500.28503CC5
First Inventor or Application Identifier	Hiroyuki MANO
Title	MULTI-TONE DISPLAY DEVICE
Express Mail Label No.	

jc535 U.S. PTO 09/625542 07/25/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)*
(Submit an original and a duplicate for fee processing)

2. [X] Specification [*Total Pages* 20]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 9]

4. Oath or Declaration [*Total Pages* 2]
a. [ ] Newly executed (original or copy)
b. [X] Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
i. [ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

** NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).*

5. [ ] Microfiche Computer Program *(Appendix)*

6. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [X] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application Status still proper and desired
14. [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. [ ] Other: .....

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
[X] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: 09/188,901
Prior application information: *Examiner* A. Mengistu *Group / Art Unit:* 2774
For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

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Name (Print/Type)	Carl I. Brundidge	*Registration No. (Attorney/Agent)*	29,621
Signature		*Date*	July 25, 2000

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500.28503CC5

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: MANO, et al

Serial No.: Not yet assigned

Filed: July 25, 2000

For: MULTI-TONE DISPLAY DEVICE

Group: 2774

Examiner: A. Mengistu

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

July 25, 2000

Sir:

The following amendments and remarks are respectfully submitted prior to the Rule 53(b) Continuation Application filed on even date.

IN THE SPECIFICATION

Please insert before the first line of the specification the following:

-- This is a continuation of application Serial No. 09/188,901, filed November 10, 1998; which is a continuation of application Serial No. 08/466,188, filed June 6, 1995; which is a continuation of application Serial No. 08/164,563, filed December 10, 1993, now abandoned; which is a continuation of application Serial No. 07/844,965, filed February 28, 1992, now U.S. Patent No. 5,298,912; which is a continuation of application Serial No. 07/475,849, filed February 6, 1990, now abandoned. --

Please amend the specification as follows:

Page 1, line 17, after "are" insert --supplied with--;

line 19, after "of" insert --the--.

Page 2, line 3, after "of" insert --the--;

line 8, delete "varies" and insert --vary--;

line 10, delete "exhibimt" and insert --exhibit--.

Page 3, line 17, delete "taken-in" and insert --display--; same line, after "data" insert --taken in--.

Page 6, line 11, delete ",".

Page 8, line 11, after "LCM" insert --is illustrated--;

line 22, delete "covnerter" and insert --converter--.

Page 9, line 1, after "generating" insert --constant--;

line 8, after "12" insert --respectively--;

line 9, delete "by one line" and insert --at a time--;

line 17, delete ";" and insert --and--;

line 18, delete "horizontal" insert --latch--;

line 26, after "circuit" insert --which--.

Page 10, line 16, delete "in" and insert --to--.

Page 11, line 1, delete "are" and insert --is--.

Page 12, line 19, after "section" insert --,--;

line 22, after "data" insert --,--.

Page 13, line 17, delete "input port of the".

Page 14, line 9, delete "from that of";

line 12, after "5" insert --to lag--.

IN THE CLAIMS

Please cancel claims 1-6 without prejudice or disclaimer of the subject matter thereof.

Please add new claims 7-15 as follows:

-- 7. A liquid crystal display device comprising:

a matrix liquid crystal display panel having a plurality of dots, each of the dots is formed with a Red (R) pixel, a Green (G) pixel and a Blue (B) pixel; and

a X direction driver having a plurality of X signal lines corresponding to each of the pixels of the matrix liquid crystal display panel, said X direction driver outputs driving voltages making the matrix liquid crystal display panel display multi-color of R, G and B,

wherein the X direction driver includes a clock terminal which receives a clock signal provided from an external device and M ports which receive M dots multi-tone digital data, each of the M dots multi-tone digital data represents driving voltages of the R, G and B, each of the R, G and B being 2^N tones, where M and N are each integers of 2 or more, and

wherein the M ports receive n dots multi-tone digital data with n/M clock pulses of the clock signal provided via the clock terminal, where n is integer of 2 or more.

8. A liquid crystal display device according to claim 7, wherein the X direction driver has output terminals, each

of the output terminals is coupled to the one of the plurality of X signal lines, and

wherein the X direction driver outputs driving voltages in accordance with the M dots multi-tone digital data.

9. A liquid crystal display device according to claim 7, wherein each of the M ports receives multi-tone digital data by one dot.

10. A liquid crystal display device comprising:

a matrix liquid crystal display panel having a plurality of dots, each of the dots is formed with a Red (R) pixel, a Green (G) pixel and a Blue (B) pixel; and

a X direction driver having a plurality of X signal lines corresponding to each of the pixels of the matrix liquid crystal display panel, said X direction driver outputs driving voltages making the matrix liquid crystal display panel display multi-color of the R, G and B,

wherein the X direction driver includes a clock terminal which receives a clock signal provided from an external device and M ports which receive M dots multi-tone digital data synchronized with the clock signal, each of the M dots multi-tone digital data being N-bit data for each of the R, G and B, each of the M multi-tone digital data represents driving voltages of the R, G and B, each of the R, G and B

displaying 2^N tones, where M and N each are an integer of 2 or more, and

wherein the M ports receive n dots multi-tone digital data with n/M clock pulses of the clock signal provided via the clock terminal, where n is integer of 2 or more.

11. A liquid crystal display device according to claim 10, wherein the X direction driver has output terminals, each of the output terminals is coupled to one of the plurality of X signal lines,

wherein the X direction driver outputs driving voltages in accordance with the M dots multi-tone digital data.

12. A liquid crystal display device according to claim 10, wherein each of the M ports receives multi-tone digital data by one dot.

13. A liquid crystal display device comprising:

a matrix liquid crystal display panel having a plurality of dots, each of the dots is formed with a Red (R) pixel, a Green (G) pixel and a Blue (B) pixel; and

a X direction driver having a plurality of X signal lines corresponding to each of the pixels of the matrix liquid crystal display panel, said X direction driver outputs driving

voltages making the matrix liquid crystal display panel display multi-color of R, G and B,

wherein the X direction driver includes a clock terminal which receives a clock signal provided from an external device and M ports which receive M dots multi-tone digital data synchronized with the clock signal, each of the M dots multi-tone digital data being N-bit data for each of the R, G and B display as 2^N tones, where M and N each are an integer of 2 or more, and

wherein the M ports receive n dots multi-tone digital data with n/M clock pulses of the clock signal provided via the clock terminal, wherein n is integer of 2 or more.

14. A liquid crystal display device according to claim 13, wherein the X direction driver has output terminals, each of the output terminals is coupled to one of the plurality of X signal lines, and

wherein the X direction driver outputs driving voltages in accordance with the M dots multi-tone digital data.

15. A liquid crystal display device according to claim 14, wherein each of the M ports receives multi-tone digital data by one dot.--

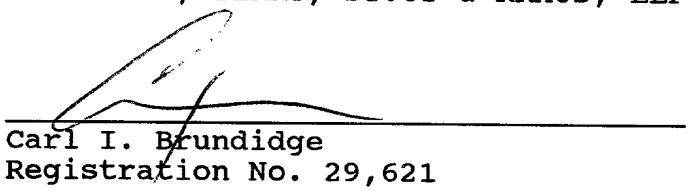
REMARKS

Entry of the above amendments prior to examination is respectfully requested.

Please charge any shortage in fees due in connection with the filing of this paper, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (500.28503CC5).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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MULTI-TONE DISPLAY DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a matrix display device, and more particularly to a device for displaying an image in plural tones in response to an analog image signal.

In recent years, matrix display devices including a liquid crystal display, a plasma display, an EL (electroluminescence), etc. have been developed as display devices in place of CRT display devices.

The display screen of the matrix display device has plural X signal lines arranged in a horizontal (X) direction of the screen, and plural Y signal lines in a vertical (Y) direction thereof; each of picture cells (pixels) is displayed at each of intersecting points of the X and Y signal lines. The X signal lines are supplied with image signals (luminance or color signals), whereas the Y signal lines are selective signals for scanning lines.

Several techniques of display for the matrix display device, which can make the display with multi-color and multi-tone as in the CRT display device, have been developed. For example, in the liquid crystal matrix display device, different tones can be exhibited in terms of different integration values of transmission light beams for liquid crystal cells. The different

integration values of transmission light beams can be exhibited by thinning out image signals for each frame of image display, or pulse-width modulating the image signals supplied to the X signals. In these techniques, the difference in time-integration values of image signals are converted into different tones. On the other hand, if the liquid crystal devices which continuously varies in their transmissivity in accordance with varying applied voltages is used, it is possible to exhibimt the tone by controlling the applied voltage.

JP-A-62-195628 filed on January 13, 1986 by HITACHI, LTD. in Japan discloses a liquid crystal display device which provides monochrome or 8 (eight)-color display in accordance with input signals which are binary digital signals. JP-A-61-75322 filed on September 20, 1984 by FUJITSU GENERAL Co. Ltd. discloses a system which provides tone display by changing signal levels between adjacent fields. JP-A-59-78395 filed October 27, 1982 by SUWA SEIKOSHA Co. Ltd. discloses a multi-tone display system using pulse-width modulation.

Now referring to Figs. 1 and 2, the operation of a liquid crystal matrix display device which does not have the function of tone display will be explained. An input signal for this matrix display device is a binary digital signal represented by the value of "0" or "1".

In Fig. 1, 1 is a liquid crystal display device (or liquid crystal display module, hereinafter

referred to as LCM) provided with a matrix shape liquid crystal panel 17 the pixels of which are selected by X signal lines and Y signal lines. 18 is display data in which display ON (white) is represented by "1" and display OFF (black) is represented by "0". 3 is a latch clock in synchronism with the display data 18. 4 is a horizontal clock indicative of the period during which the amount of display data corresponding to one horizontal display is sent. 5 is a head line signal. 19 is a voltage generating section. 20 is a display ON voltage. 21 is a display OFF voltage. 13 is a selected voltage. 14 is a non-selected voltage. These voltages are generated by the voltage generating section. 22 is an X driving section for driving X-signal lines which is reset by the trailing edge of the horizontal clock, takes in the display data 18 corresponding to one horizontal display, converts the taken-in data into a display ON voltage for the data "1" and into a display OFF voltage for the data "0", and finally outputs the converted voltage in accordance with the next trailing edge of the horizontal clock 4. X1 - X640 are panel data which are output voltages from the X driving section. 16 is a Y driving section for driving Y signal lines. Y1 - Y200 are scanning signals. The Y driving section 16 takes in the head line signal in accordance with the trailing edge of the horizontal clock 4, initially takes the scanning signal Y1 as the selected voltage 13, and shifts the selected voltage 13 in the

order of scanning signals Y2, Y3, ... Y200 (each of the scanning signals other than the scanning signal which is a selected voltage 13 is a non-selected voltage 14). The liquid crystal panel 17 displays data on the line corresponding to the scanning signal Y1 which is at the level of the selected voltage in accordance with the panel data X1 - X640 which are X-signal-line driving voltages X1 - X640 generated from the X driving section 22.

Fig. 2 is a timing chart for explaining the operation of the LCM 1.

In Fig. 1, the X driving section 22 successively takes in the display data for each one line in synchronism with the latch clock 3 and in accordance with the subsequent horizontal clock 4, outputs as panel data X1 - X640, the display ON voltage 20 or the display OFF voltage selected by "1" or "0" of each data. As shown in Fig. 2, therefore, the X driving section 22 outputs the voltage selected by the data for a 200-th line which is a last line while taking in a first line data, and outputs the voltage selected by the first line data while taking in a second line data. Namely, the output of display data lags by one line from the take-in thereof. Then, in order that the scanning signal on the line to be output by the X driving section 22 is the selected voltage, the Y driving section 16 takes in the head line signal 5 at the timing of the horizontal clock 4, takes the scanning signal Y1 as the selected voltage

13 and thereafter shifts the selected voltage 13 in accordance with the horizontal clock 4. In accordance with the voltage of each of the panel data X1 - X640, the display panel 17 displays "white", on the line corresponding to the scanning line which is the selected voltage, when it is the display ON voltage and displays "black" when it is the display OFF data.

Color display (8 color display) can be made by arranging color filters of red, green and blue in the direction of lines (Y direction) or the direction of dots (X direction), and additively mixing three dots (3 bit data) constituting one dot (pixel) of visible information through display ON or OFF thereof.

Meanwhile, development of multi-color and multi-tone display in accordance with the demand for multi-color display and multi-tone display gave rise to a problem of interface between information processing devices such as between a liquid crystal panel and a personal computer. More specifically, if 4096 colors are to be displayed, signal lines corresponding to 4 bits are required for each of R (red), G (green) and B (blue) so that a total of 12 signal lines are required. Further, if 32768 colors are to be displayed, signal lines corresponding to 5 bits (total of 15 signal lines) are required for each of R, G and B. Increase in the number of signal lines will complicate the interface between e.g. the display panel and the personal computer and give rise to unnecessary radiation. This can be

prevented by using analog input signal lines.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a new matrix display device in a multi-tone display system which is different from the conventional matrix display systems.

In the display device according to an embodiment of the present invention, an analog signal is used as an input signal. The analog signal is A-D converted into a digital signal. A voltage generating device is provided to generate, plural voltages in accordance with tones to be displayed. An output voltage from the voltage generating device is selected in accordance with the value represented by the digital signal. The selected voltage is applied to a display element to display a desired tone.

A matrix display device according to an embodiment of the present invention comprises a matrix display panel having a matrix composed of plural X direction signal lines and plural Y direction signal lines lying at right angles thereto, intersecting points on the matrix being pixels of an image to be displayed, an X direction driving section for sequentially scanning the X direction signal lines to provide image signals, a Y direction driving section for the Y direction signal lines in synchronism with the scanning of the X direction signal lines to sequentially provide select

signals to the Y direction signal lines, an A-D converter section for receiving an analog signal and converting it into a digital signal, a voltage generating section for generating signals at plural voltage levels, and a selector section for selecting an output signal from the voltage generating section in accordance with the output from A-D converter section and providing it to the X direction driving section as an image signal.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a liquid crystal matrix display device for displaying an image in response to a digital signal input;

Fig. 2 is a waveform chart for explaining the operation of the display device of Fig. 1;

Fig. 3 is a block diagram of a liquid crystal matrix display device according to a first embodiment of the present invention;

Fig. 4 is a block diagram of an example of the X driving section of Fig. 3;

Fig. 5 is a block diagram of an embodiment of a liquid crystal matrix display device (LCM) for color display according to the present invention;

Fig. 6 is a block diagram of the main part of LCM according to the second embodiment of the present invention;

Fig. 7 is a timing chart for explaining the

operation of the serial-parallel converter means of Fig. 6;

Fig. 8 is a block diagram of an input part of the parallel X driving section of Fig. 6; and

Fig. 9 is a block diagram of the main part of another embodiment of a liquid crystal matrix display device for color display according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now referring to Figs. 3 and 4, an embodiment of a multi-tone display LCM according to the present invention. In this embodiment, it should be noted that an analog display data or signal (stepwise analog signal) 2 having different voltage levels corresponding to the number N of tones to be displayed is input to the display device. For simplicity of explanation, it is assumed that N = 4, the analog input signal is represented by the voltage levels corresponding to 4 (four) tones. The analog signal is sent from an image display output of e.g. a personal computer. In Fig. 3, 6 is an A-D converter section; 7 is a digital display data. The A-D covnerter section 6 converts the analog display data 2 as an input into the digital display data which is represented by 2 bits; more specifically, four value voltage levels of the analog display data are converted into (0, 0), (0, 1), (1, 0), and (1, 1) from the lower levels. 8 is a multi-voltage-level output generating

circuit for generating voltages at plural levels in accordance with tones to be displayed, e.g. voltages at four different levels since this embodiment is directed to 4 tone display. The signal at the voltage level corresponding to tone 0 is output to a signal line 9. The signals at voltage levels corresponding to tone 1, tone 2 and tone 3 are output to signal lines 10, 11, and 12. 15 is an X driving section which takes in 2 bit digital data 7 sequentially one line by one line in synchronism with the latch clock 3, selects one of the four tone voltages output to the signal lines 9, 10, 11 and 12 in accordance with the decoded value of data for each dot and outputs it as panel data X1 - X640. The remaining reference numbers denote like parts in Fig. 1.

Fig. 4 shows an example of the X driving section shown in Fig. 3. In Fig. 4, 23 is a latch selector; S1 - S640 are select signals. The latch selector 23 is cleared by horizontal clock 3 and sequentially boosts the select signals S1, S2, ... S640 "high" in synchronism with the succeeding clocks 3. 24 is a latch circuit which serves to latch the digital display data 7 in blocks (latch 1 - latch 640) in which the select signal is "high". 25 to 28 are outputs from the respective blocks of the latch circuit 24, i.e. 2 bit latch data 1 to 640. 29 is a horizontal latch circuit latches the latched data 1 to 640 in horizontal latches 1 to 640 in synchronism with the horizontal clock 4. 30 to 33 are outputs from the respective

blocks of the horizontal latch circuit 29, i.e. 2 bit horizontal data 1 to 640. 34 is a decoder which serves to decode the horizontal data 1 to 640 by the corresponding decoder blocks (decoders 1 to 640). Numerals 35 to 38 are outputs from the decoder blocks, i.e. decoded values 1 to 640. Numeral 39 indicates a voltage selector which serves to select one of the tone voltages in accordance with the decoded values 1 - 640.

Now referring to Figs. 3 and 4, the operation of the multi-tone display LCM 1 shown in Fig. 3 will be explained. In Fig. 3, the analog display data 2 is converted into the 2 bit digital data 7 by the A-D converter section 6; the 2 bit digital display data 7 is input to the X driving section 15. The X driving section 15 takes the display digital data 7, in synchronism with the latch clock 3 (Fig. 2), in one latch block of the latch circuit 24 to which a "high" select signal is being input. The latch selector 23 shifts the "high" state of the select signal each time the latch clock 3 is input. The latch circuit 24 takes in the sequentially sent digital display data 7 in the latch blocks 1, 2, ... 640. When the latch circuit 24 has taken in the digital display data 7 corresponding to one line, i.e. up to latch block 640, the horizontal clock (Fig. 2) is applied to the X driving section 15 to clear the latch selector 23; then the X driving section stands by for next take-in of the digital display data 7. The data latched by the latch circuit

24 are sent to the horizontal latch circuit 29 which latches the data from the latch circuit 24 in synchronism with the horizontal clock 4 (Fig. 2). The horizontal data 30 to 33 which are outputs from the horizontal latch circuit 29 are sent to the decoder 34 and decoded by the decoder blocks 1 to 640 thereof; the decoded values 35 to 38 are output from the decoder 34. In the voltage selector 39, the selector blocks 1 to 640, in accordance with the decoded values, selects tone 0 voltage 9 if the decoded value is "0", tone 1 voltage 10 if it is "1", tone 2 voltage 11 if it is "2", and tone 3 voltage 12 if it is "3". The tone voltages output from the voltage selector blocks are sent to the liquid crystal panel 17 as panel data X1 to X640. Thus, the four value voltages output from the X driving section 15 are applied to the liquid crystal elements corresponding to the line selected by the Y driving section 16 in response to the select voltage 13 sent from the voltage generating circuit 8. In this way, the LCM 1 shown in Fig. 3 can realize four tone display.

Although the four tone display has been adopted in this embodiment, 2^N tone display can be realized. More specifically, if the input analog display data is represented by 2^N (N is an integer of 1 or more) levels, it is converted into N bit digital data by the A-D converter section 6, the data width in the internal circuits in the X driving circuit 15 is set at N bits, and 2^N kinds of tone voltage are supplied to the

X driving section 15 to display 2^N tones.

Now referring to Fig. 5, one embodiment of the LCM for multi-color display will be explained. The multi-color display can be realized by arranging color filters of R (red), G (green) and B (blue) in the direction of dots on the liquid crystal panel 17, providing A-D converter sections 43, 44 and 45 for R40, G41 and B42 as input analog display data, and applying the outputs from the R, G and B A-D converter sections 43, 44 and 45 to a color X driving section 46. In this case, the color X driving section 46 has three columns of the arrangement shown in Fig. 4 and thus the corresponding panel data are RX1 - RX640, GX1 - GX640 and BX1 - BX640.

With reference to Figs. 6 to 8, another embodiment of the multi-tone LCM will be explained. In this embodiment, it should be noted that a parallel input of M (M is a positive integer) dots are applied to the X driving section and it is assumed that M = 2.

In Fig. 6, like reference numerals denote like elements in Fig. 3. 47 is a serial-parallel converter section. 48 is a first dot digital data and 49 is a second dot digital data. The serial-parallel converter section 47 converts 2 bit serial digital data 7 from the A-D converter section 6 into a parallel data consisting of the first dot digital data 48 and the second dot digital data 49, each data consisting of 2 bits. 50 is a timing correction section. 51 is a parallel clock.

52 is a correction horizontal clock. 53 is a correction head line signal. In response to the latch clock 3, the timing correction section 50 generates a parallel clock 51 in synchronism with the parallel data consisting of the first dot digital data 48 and the second dot digital data 49. Further, in order to correct the phase deviation of data due to the serial-parallel conversion of the display data, the timing correction section 50 corrects the horizontal clock 4 and the head line signal 5 using the latch clock 3 to provide a corrected horizontal clock 52 and a corrected head line signal 53. 54 is a parallel X driving section which serves to sequentially take in the 2 bit parallel display data in synchronism with the parallel clock 51.

Fig. 7 is a timing chart showing the operation of the serial-parallel conversion section 47. Fig. 8 is a block diagram of the input port of the parallel X driving section 54. In Fig. 8, 55 is parallel latch select which is cleared by the corrected horizontal clock 52 and thereafter sequentially boosts select signals S1, S2, ... S320 to "high". 56 is a parallel latch circuit; the latch block thereof for which the select signal is "high" latches simultaneously the first dot digital data 48 and second dot digital data 49 at the timing of the parallel clock 51. The other reference numerals in Fig. 8 denote like elements in Fig. 4.

The operation of the multi-tone LCM shown in

Fig. 6 will be explained. The analog display data 2 having four value voltage levels is the 2 bit digital display data 7 by the analog-digital converter section 6. This digital display data 7 is converted into 2 bit parallel data, as shown in Fig. 7, to provide the first dot digital data 48 and second dot digital data 49 which are in synchronism with the parallel clock 51. Then, as shown in Fig. 7, owing to the serial-parallel conversion, the phase of the output data lags from that of the input data by 2 (two) latch clocks 3. In order to correct this lag, the timing correction section 50 also causes the horizontal clock 4 and the head line signal 5 by 2 latch clocks 3. The resulting corrected horizontal clock 52 and corrected head timing signal 53 are applied to the X driving section 54 and the Y driving section 16. As seen from Fig. 8, the X driving section 54 takes the first dot digital data 48 and the second dot digital data 49, in synchronism with the parallel clock 51, into its one block to which the "high" select signal is applied from the parallel latch select 55. The parallel latch select 55 is cleared by the corrected horizontal clock 52 and thereafter sequentially boosts the select signals S1 to S320 to "high". Thus, the parallel latch circuit 52 also latches the data in the order of latch blocks 1, 2, ... 320 to finally latch the data corresponding to one line. The outputs from the blocks of the parallel latch circuit 56 are latched in the horizontal latch circuit 52 at the timings of the

corrected horizontal clock 52. The following operation is the same as that in Fig. 4. Thus, parallel data X1 to X640 are provided as panel data.

As understood from the above explanation, two dots can be used as an input to the X driving section 46 by providing the serial-parallel conversion section 47, causing the internal port of the X driving section 46 to simultaneously latch two dots and providing the timing correction section for correcting the phase lag due to the serial-parallel conversion. This can enhance the operation speed of the circuits successive to the A-D converter section 6. In another embodiment of the invention, the timing correction section 50 is not required when the input timing is determined in consideration of the phase delay in the serial-parallel conversion section 47 (two latch clocks 3) so that the horizontal clock 4 and the head line signal 5 can be directly used without correction. Incidentally, although in this embodiment, the input to the X driving was 2 bits for each of 2 dots, the input of N bit(s) (N is an integer of 1 or more) for each of M dots (M is an integer of 2 or more) can be realized in the same way.

A second embodiment of the LCM for color display as shown in Fig. 9 can be realized by providing R, G and B serial-parallel converter sections 57, 58 and 59, and providing a color parallel X driving section 60 with three columns of the arrangement of Fig. 8.

Further, although the explanation hitherto

made was directed to a liquid crystal display device, the same idea can be also applied to the other display devices such as a plasma display, EL display, etc.

In accordance with the present invention, an LCM for multi-tone display or multi-color can be realized thereby to decrease the number of input lines to LCM. Moreover, by using an analog input to decrease the number of data bits, noise to be generated can be reduced. Further, by carrying the parallel operation of the X driving section, the operation speed can be enhanced. Furthermore, since the voltages in accordance with N bit decoded values can be selected as outputs from the X driving section, tone voltage with less fluctuation can be provided.

CLAIMS:

1. An image display device comprising:

a matrix display panel having plural X direction signal lines and plural Y direction signal lines intersecting lying at right angles thereto, the intersecting points of said matrix being pixels of a display image;

X direction driving means for sequentially scanning said plural X direction signal lines to provide image signals;

Y direction driving means for driving said plural Y signal lines in synchronism with the scanning of said plural X direction signal lines to sequentially provide, select signals to said plural Y direction signal lines;

A-D converter means for receiving an analog image signal and converting it into a digital image signal;

voltage generating means for generating signals at plural different voltage levels; and

selector means for selecting one of the output signals from said voltage generating means in accordance with an output from said A-D converter means to provide it to said X direction driving means as said image signal.

2. An image display device according to claim 1, wherein said matrix display panel comprises a liquid crystal display panel.

3. An image display device according to claim 1, wherein said matrix display panel comprises a plasma display panel.

4. An image display device according to claim 2, wherein said liquid crystal panel comprises liquid crystal cells capable of distinguishably displaying information of N (N: positive integer) for one pixel, and said voltage generating means generates signals at different 2^N kinds of voltage levels.

5. An image display device according to claim 2, wherein said liquid crystal panel comprises display elements radiating N (N: positive integer) kinds of colors for one pixel, said X direction signal lines comprises 2^N signal lines corresponding to said N kinds of different colors, and said A-D converter means comprises means for receiving N kinds of different color image analog signals and converting them into N kinds of different color image digital signals.

6. An image display device according to claim 1, wherein said A-D converter means converts said analog input signal into an M (M: positive integer) bit parallel digital signal to be supplied to said selector means.

ABSTRACT OF THE DISCLOSURE

This specification discloses a novel multi-tone display matrix display device. The matrix display device according to an embodiment of the present invention comprises a matrix display panel having a matrix composed of plural X direction signal lines and plural Y direction signal lines lying at right angles thereto, intersecting points on the matrix being pixels of an image to be displayed, an X direction driving section for sequentially scanning the X direction signal lines to provide image signals, a Y direction driving section for driving the Y direction signal lines in synchronism with the scanning of the X direction signal lines to sequentially provide select signals to the Y direction signal lines, an A-D converter section for receiving an analog signal and converting it into a digital signal, a voltage generating section for generating signals at plural voltage levels, and a selector section for selecting an output signal from the voltage generating section in accordance with the output from A-D converter section and providing it to the X direction driving section as an image signal.

FIG. 1

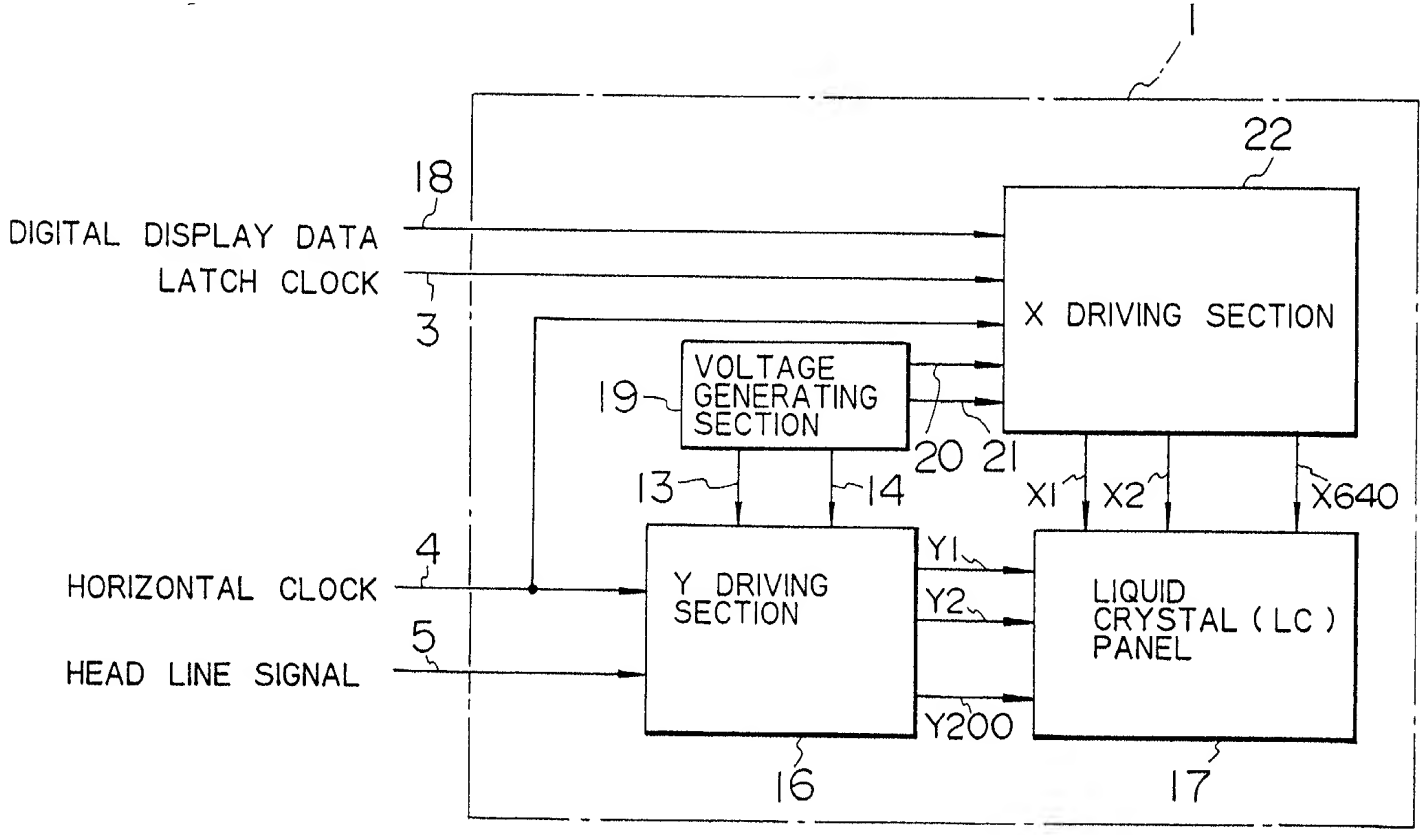


FIG. 2

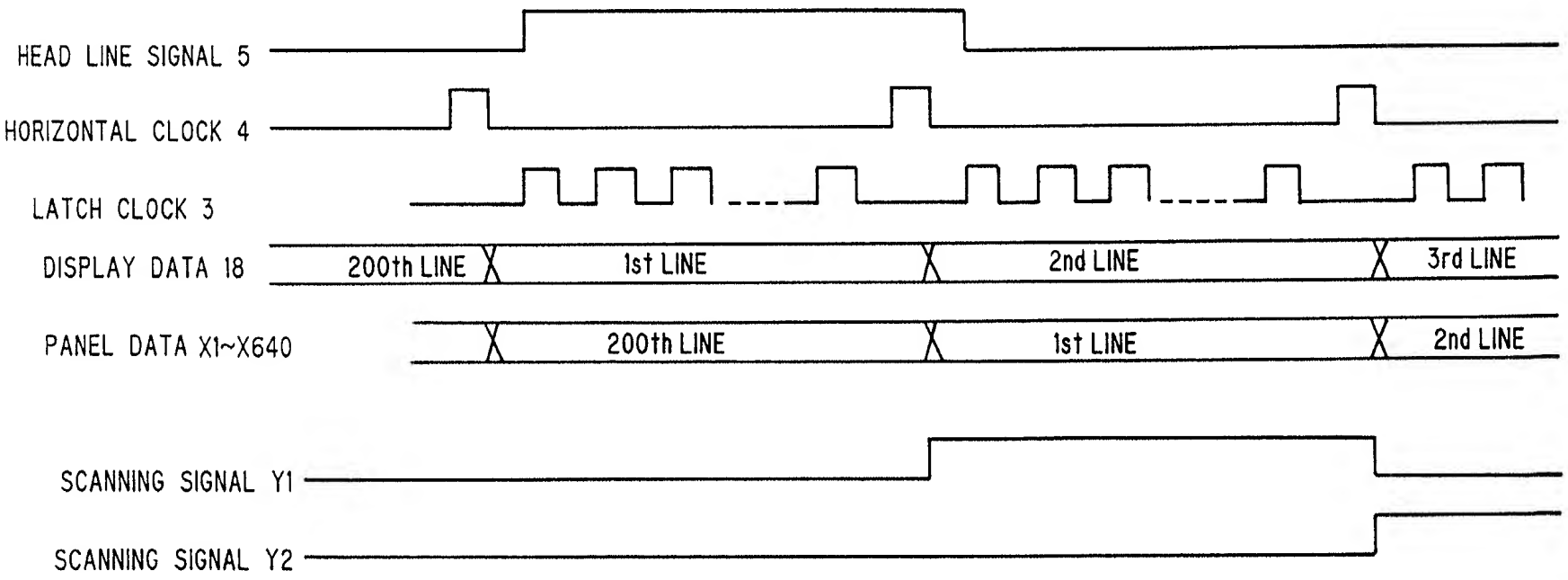


FIG. 3

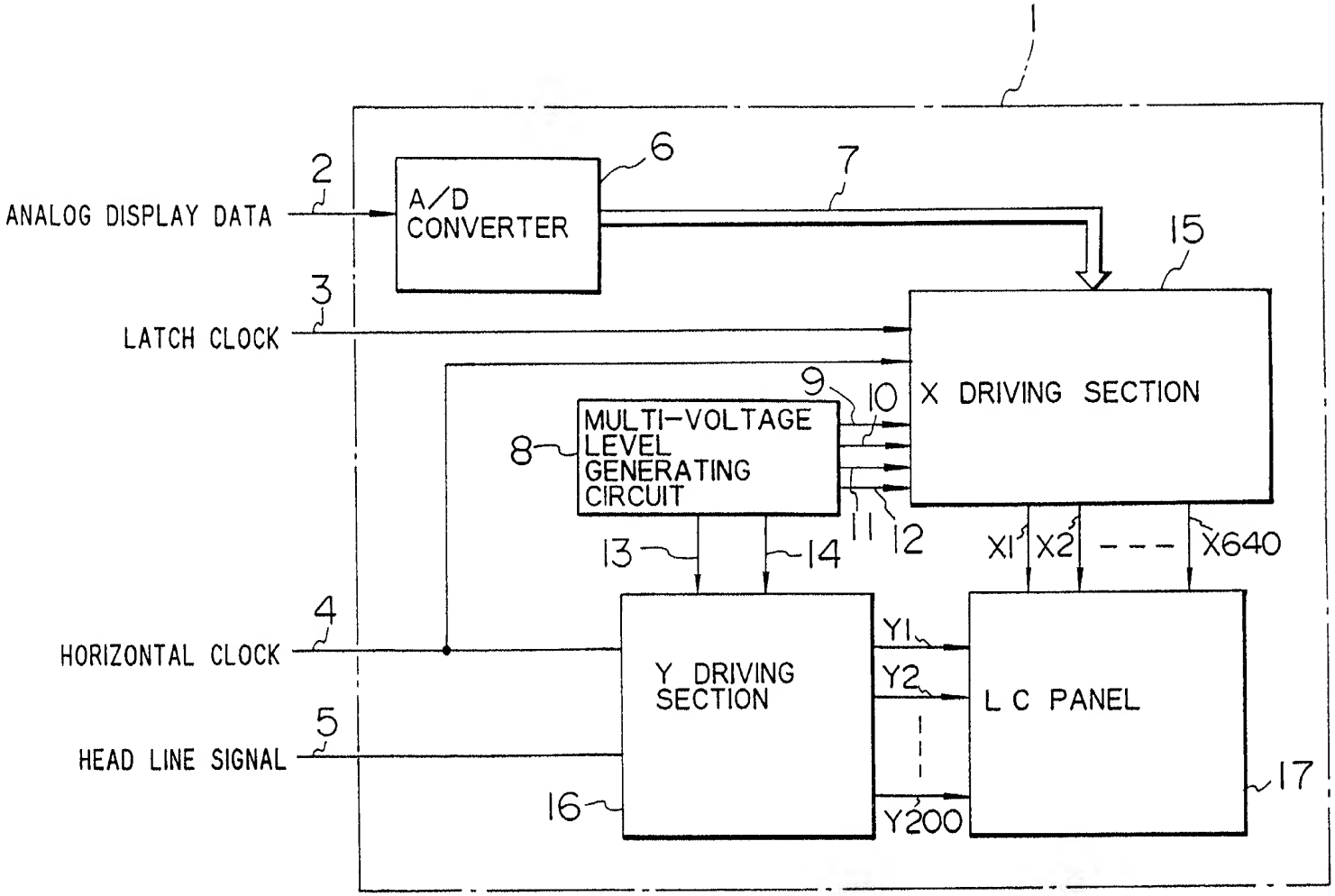

1
2
ANALOG DISPLAY DATA
A/D CONVERTER
6
7
15
3
LATCH CLOCK
X DRIVING SECTION
9
10
8
MULTI-VOLTAGE LEVEL GENERATING CIRCUIT
11
12
13
14
X1
X2
X640
4
HORIZONTAL CLOCK
Y DRIVING SECTION
Y1
Y2
Y200
L C PANEL
5
HEAD LINE SIGNAL
16
17

FIG. 4

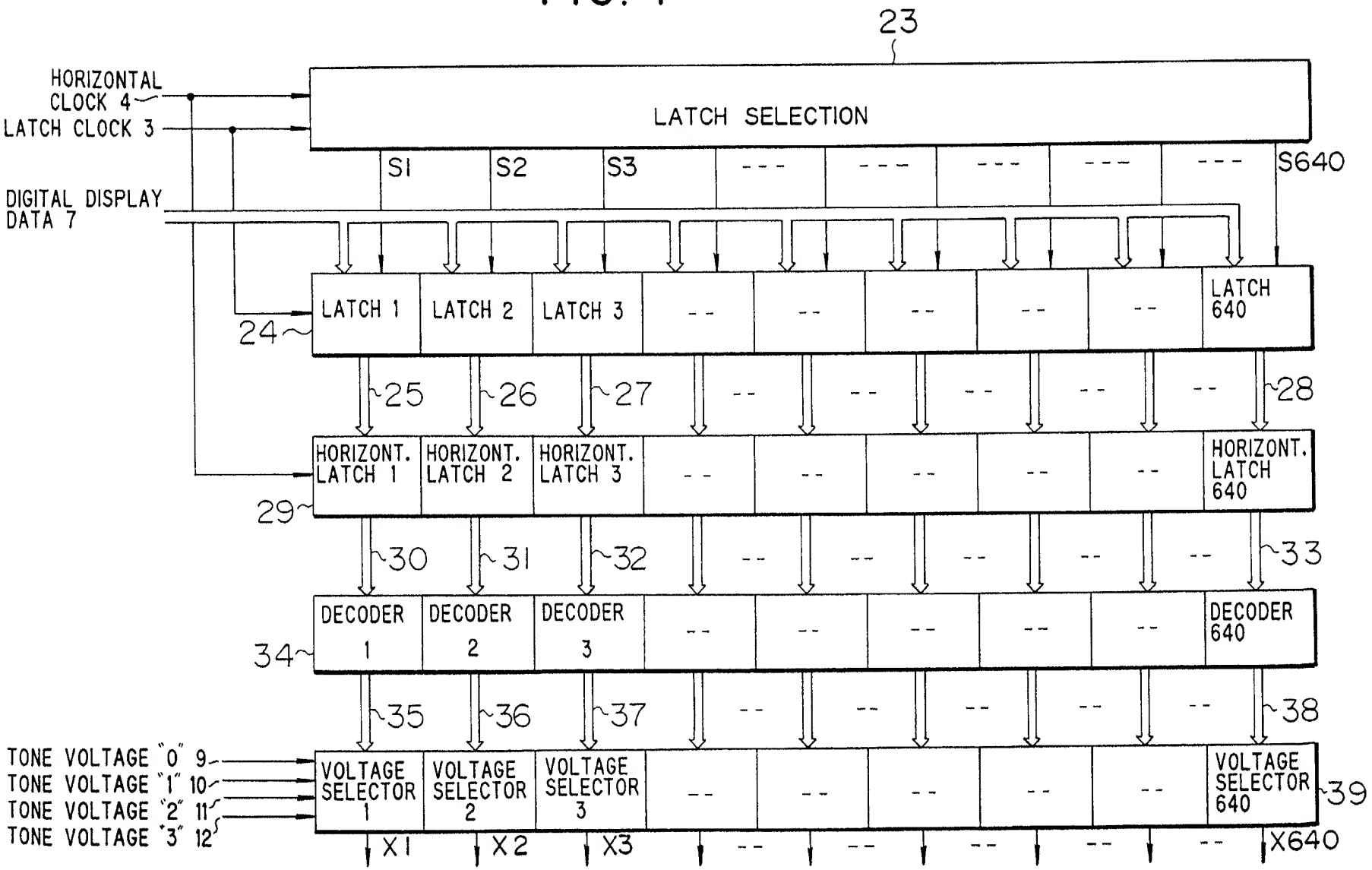


FIG. 5

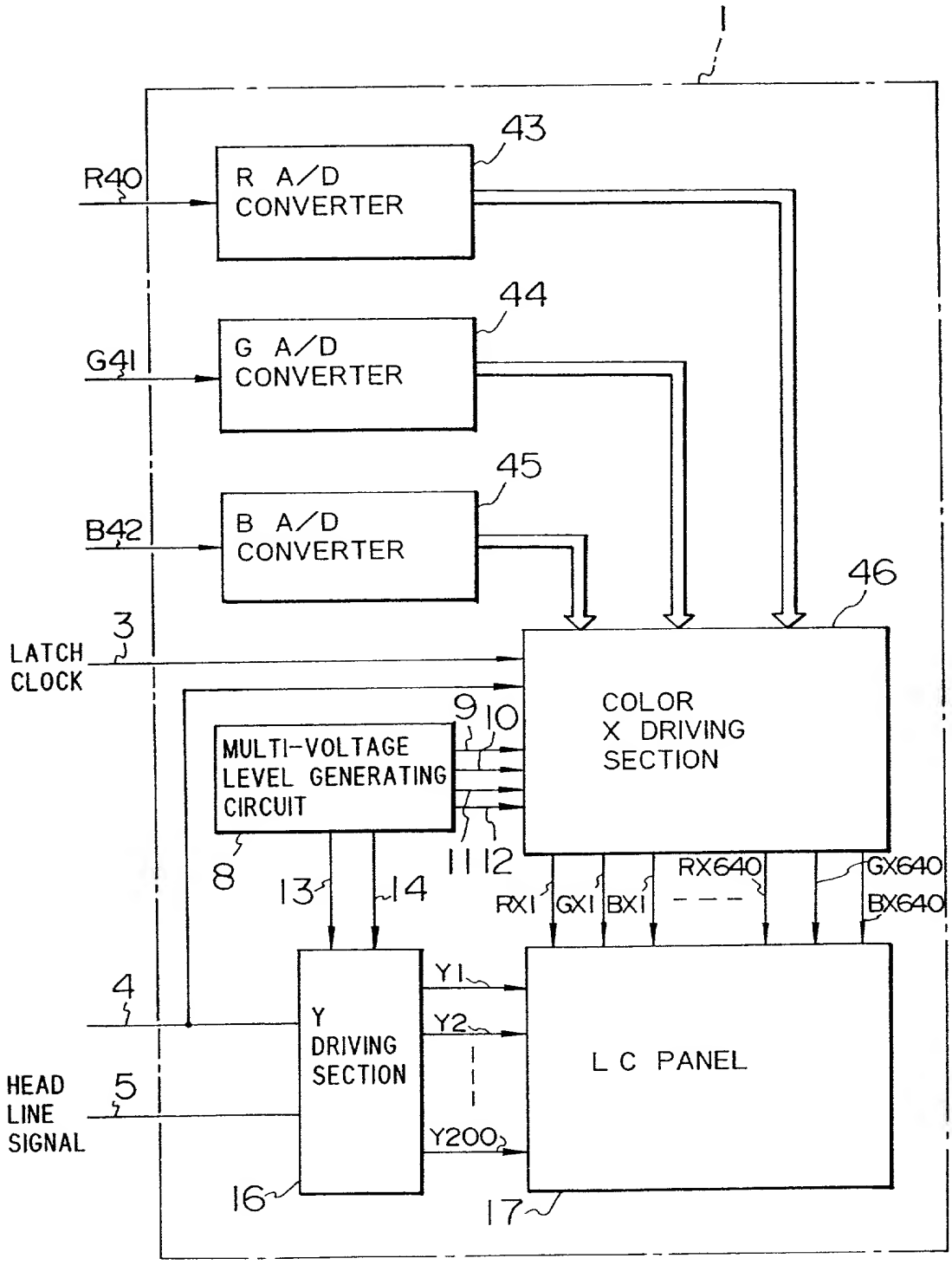

1
43
R40
R A/D CONVERTER
44
G41
G A/D CONVERTER
45
B42
B A/D CONVERTER
46
3
LATCH CLOCK
9
10
MULTI-VOLTAGE LEVEL GENERATING CIRCUIT
COLOR X DRIVING SECTION
8
11
12
13
14
RX1
GX1
BX1
RX640
GX640
BX640
4
Y DRIVING SECTION
Y1
Y2
Y200
L C PANEL
HEAD LINE SIGNAL
5
16
17

FIG. 6

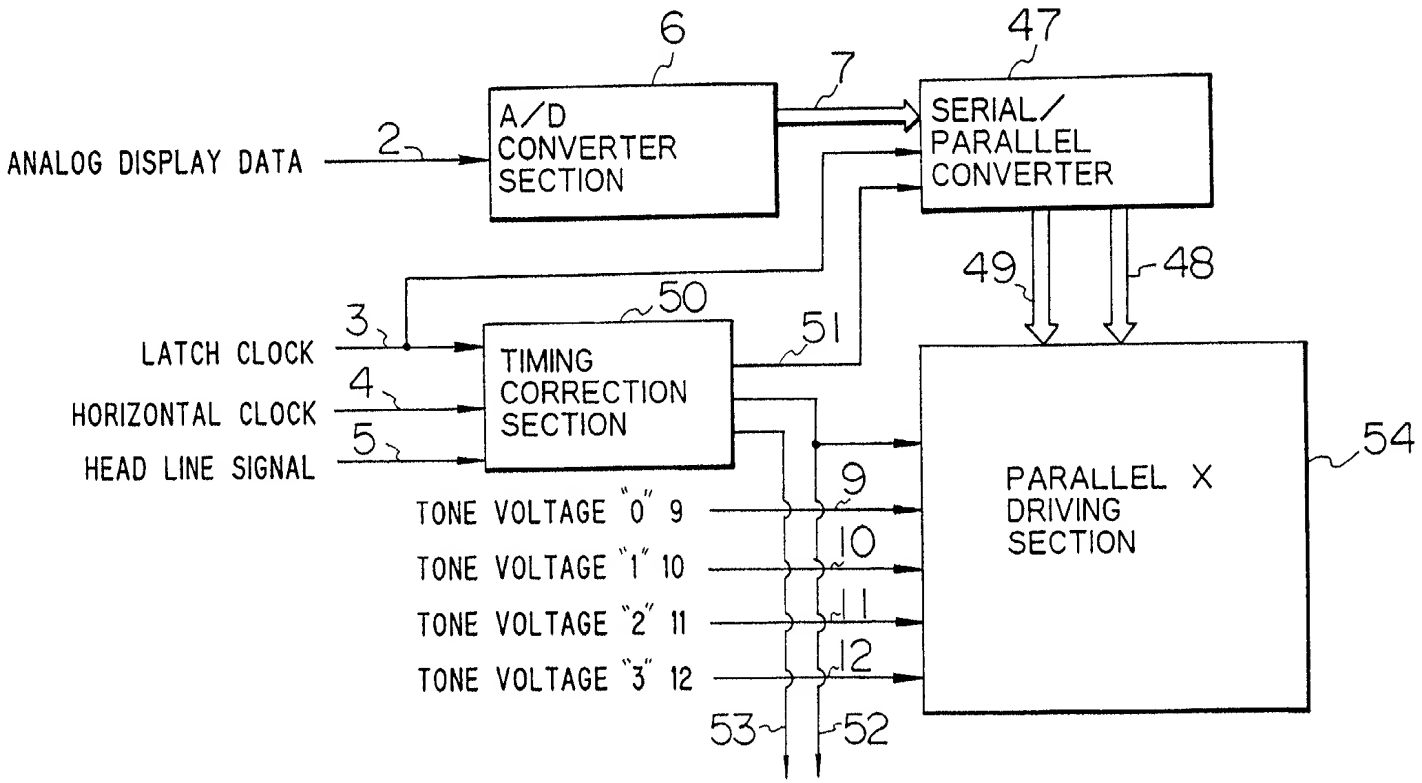

6
47
7
ANALOG DISPLAY DATA
2
A/D CONVERTER SECTION
SERIAL/ PARALLEL CONVERTER
49
48
50
3
LATCH CLOCK
4
HORIZONTAL CLOCK
5
HEAD LINE SIGNAL
TIMING CORRECTION SECTION
51
54
9
TONE VOLTAGE "0" 9
10
TONE VOLTAGE "1" 10
11
TONE VOLTAGE "2" 11
12
TONE VOLTAGE "3" 12
PARALLEL X DRIVING SECTION
53
52

FIG. 7

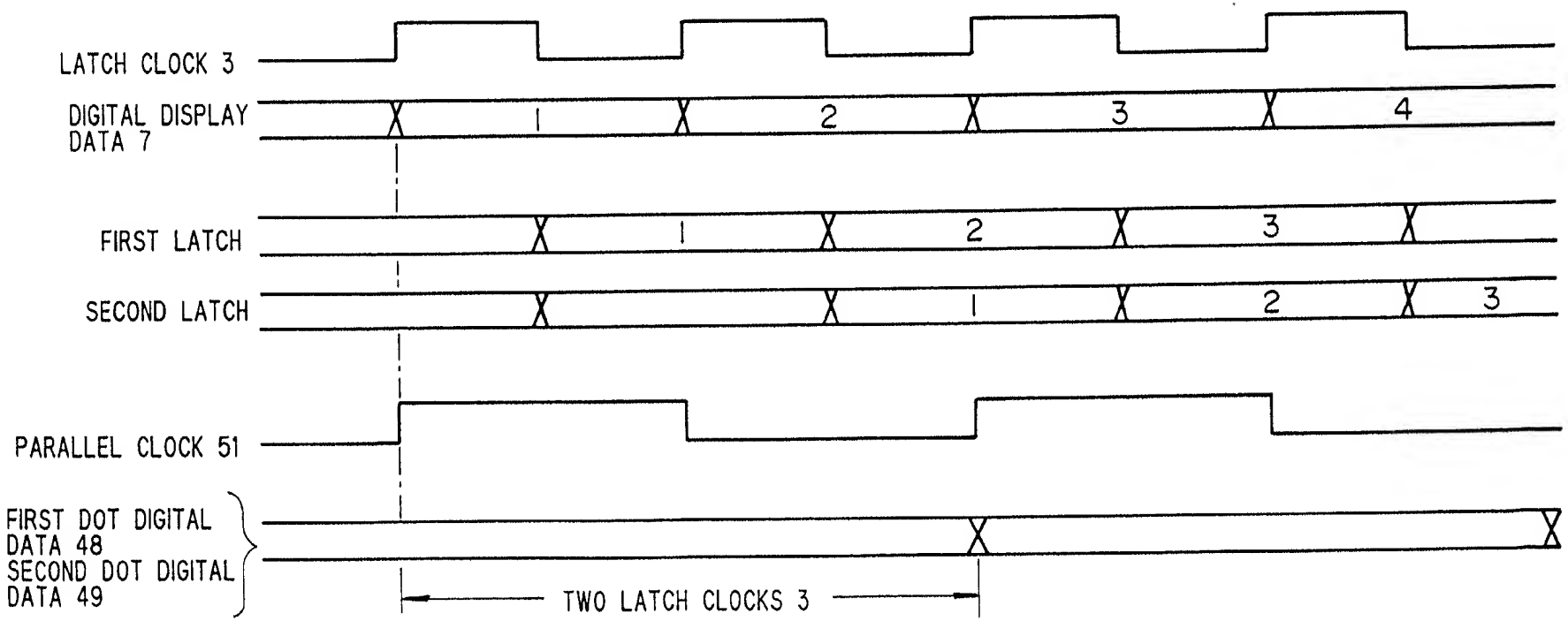


FIG. 8

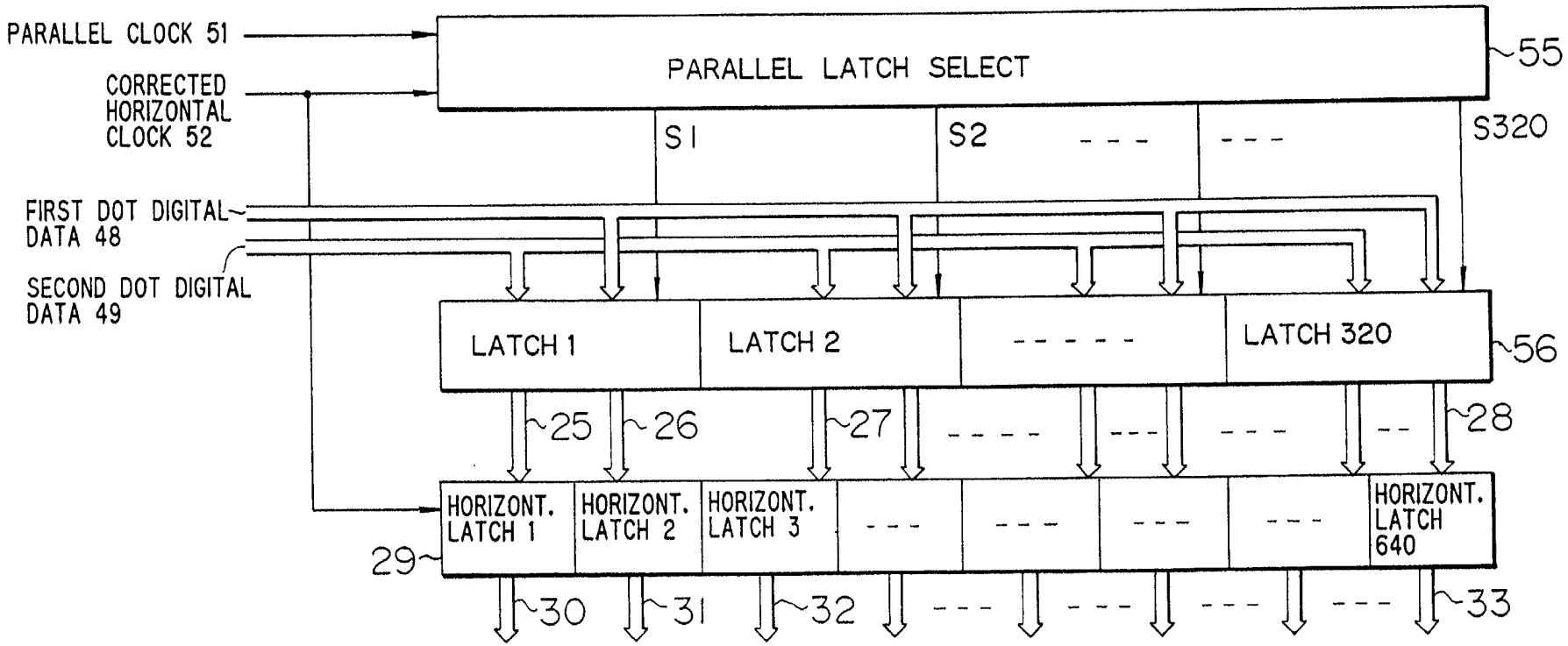
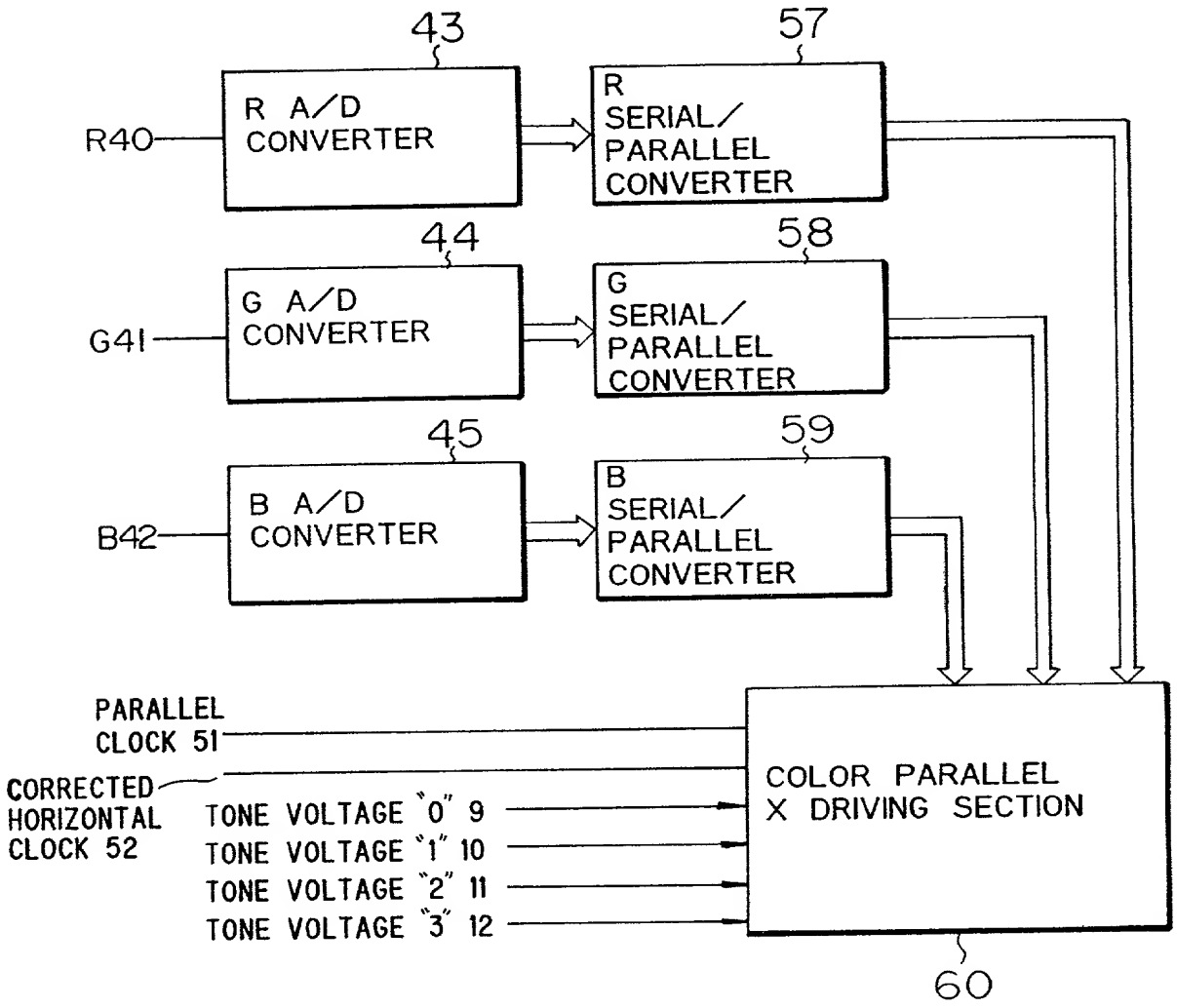


FIG. 9


43
57
R40
R A/D CONVERTER
R SERIAL/ PARALLEL CONVERTER
44
58
G41
G A/D CONVERTER
G SERIAL/ PARALLEL CONVERTER
45
59
B42
B A/D CONVERTER
B SERIAL/ PARALLEL CONVERTER
PARALLEL CLOCK 51
CORRECTED HORIZONTAL CLOCK 52
TONE VOLTAGE "0" 9
TONE VOLTAGE "1" 10
TONE VOLTAGE "2" 11
TONE VOLTAGE "3" 12
COLOR PARALLEL X DRIVING SECTION
60

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COMBINED DECLARATION AND POWER OF ATTORNEY
(宣誓書及び委任状)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name, I believe I am the original, first and sole inventor (if only one name is listed bleow) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

"MULTI-TONE DISPLAY DEVICE"

the specification of which: (check one) ☒ is attached hereto.

☐ was filed on _____
as Application Serial No. _____
and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amedment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
01-066102 (Number)	Japan (Country)	20 March, 1989 (Day/Month/Year Filed)	☒ Yes	☐ No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐ Yes	☐ No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐ Yes	☐ No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

_____ (Application Serial No.)	_____ (Filing Date)	_____ (Status) (patented, pending, abandoned)
_____ (Application Serial No.)	_____ (Filing Date)	_____ (Status) (patented, pending, abandoned)

(Continued on Page 2)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Date _____ Inventor _____

Residence _____ Citizenship _____

Post Office Address _____